show the changes made pursuant to 37 CFR 1.121(c)(1)(ii) is attached hereto as Appendix A.

Claim 11. (Twice Amended) A PLL frequency synthesizer which outputs a signal having a desired frequency, comprising:

a voltage-controlled oscillator (VCO) for generating an output signal having ~~and~~ a frequency;

C1

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator and for driving the VCO, wherein the voltage of the output signal from the charge pump is within predetermined driving limits, and

wherein when the charge pump output signal voltage changes to a value close to one of the driving ~~lim~~its thereof, both the output signal from the charge pump and a power supply signal independent of the charge pump and having a voltage which cancels the change in the charge pump output signal voltage are inputted to the VCO, thereby maintaining stability of the output signal from the VCO.

Claim 12. (Amended) A PLL frequency synthesizer which outputs a signal having a set frequency, comprising:

C2

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

C2 cont.

a charge pump for producing an output signal in response to the difference signal output from the phase comparator,

wherein the VCO is driven by the output signal from the charge pump and a power supply signal independent of the charge pump and having a voltage controlled based on the set frequency, to thereby widen an apparent lock range of the PLL.

Claim 13. (Twice Amended) A radio communication apparatus comprising a PLL frequency synthesizer which outputs a signal having a desired frequency, the PLL frequency synthesizer including:

C3

a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator and for driving the VCO, wherein the voltage of the output signal from the charge pump is bound within predetermined driving limits, and

wherein when the charge pump output signal voltage changes to a value close to one of the driving limits thereof, both the output signal from the charge pump and a power supply signal independent of the charge pump and having a voltage which cancels the

C3 Cancel. change in the charge pump output signal voltage are inputted to the VCO, thereby maintaining stability of the output signal from the VCO.

Claim 14. (Amended) A radio communication apparatus comprising a PLL frequency synthesizer which outputs a signal having a set frequency, the PLL frequency synthesizer including:

C4

a voltage-controlled oscillator (VCO) for generating an output signal having voltage and a frequency;

a phase comparator for comparing a phase of the frequency of the VCO generated output signal with a phase of a frequency of a reference signal and outputting a difference signal; and

a charge pump for producing an output signal in response to the difference signal output from the phase comparator,

wherein the VCO is driven by the output signal from the charge pump and a power supply signal independent of the charge pump and having a voltage controlled based on the set frequency, to thereby widen an apparent lock range of the PLL.